

ABSTRACT OF THE DISCLOSURE

A memory device with multiple clock domains. Separate clocks to different portions of the control circuitry create different clock domains. The different domains
5 are sequentially turned on as needed to limit the power consumed. The turn on time of the domains is overlapped with the latency for the memory access to make the power control transparent to the user accessing the memory core. The memory device can dynamically switch between a fast and a slow clock depending upon the needed data bandwidth. The data bandwidth across the memory interface can be
10 monitored by the memory controller, and when it drops below a certain threshold, a slower clock can be used. The clock speed can be dynamically increased as the bandwidth demand increases.